Serial No.: 10/689,923
Group Art Unit: 2823

REMARKS

Allowable Subject Matter

The Examiner stated that claims 7–10 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 7 has accordingly been rewritten in independent form to include all of the limitations of independent claim 6 from which it depended, and is therefore now believed to be in condition for allowance. Claims 8–10 depend from claim 7 and are therefore similarly believed to be in condition for allowance.

Allowance of claims 7-10 is accordingly respectfully requested.

Election/Restrictions

The Examiner acknowledged Applicants' election of claims 1–10 in the reply filed on March 30, 2005 and stated that since the Applicants did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse.

Applicants have elected claims 1–10, but respectfully submit for the record that the Applicants' election in response to the Restriction Requirement was with traverse and without waiving any rights for reconsideration of claims 1–10 or of filing a continuation or divisional application.

Further, it is respectfully pointed out that the process of making and the product are not believed to be patentably distinct, and that the search and examination of the invention can be performed without "serious burden". Notwithstanding the Examiner's earlier explanation, it is also pointed out that it is now established and common practice for Examiners in the United States Patent and Trademark Office ("USPTO") regularly and without objection to perform searches – in a single application – on related method and device claims in applications filed in the USPTO under the Patent Cooperation Treaty ("PCT"). This practice is in conformance with the requirements of PCT Rule 13, and because the USPTO is a PCT receiving office, the USPTO is bound by the PCT Rules. The restriction

requirement in the present application is not in conformity therewith and therefore cannot and should not have been maintained following the Applicants' traversal thereof.

For these reasons, it is believed that the Restriction requirement was improper, and withdrawal thereof is respectfully requested.

Claim Rejections - 35 USC §102

Claims 1-5 are rejected under 35 U.S.C. 102(a) as being anticipated by Watt (U. S. Patent 6,586,296 B1, hereinafter "Watt").

Watt provides a method of doping dual-gate CMOS technology wells, channels, and gates using a reduced number of masks. Wells of opposite conductivity type are formed using a single patterned layer. A silicon layer having first and second portions of opposite conductivity type may be formed using a single patterned layer or an additional patterned layer. Channel dopant regions of opposite conductivity type may be formed within the wells. Impurities may be introduced at varying energies and doses to compensate for the introduction of subsequent impurities. A dual gate transistor pair, including n-channel and p-channel transistors, may be formed.

Regarding claim 1, this claim has been amended to incorporate thereinto the subject matter of claims 3 and 4, and therefore, claims 3 and 4 have been canceled without prejudice. Accordingly, the rejection of claim 1 will be discussed comprehensively below within the context of the rejection of claims 3 and 4.

The Applicants respectfully traverse the rejection of claim 1 since the Applicants' claimed combination now includes the limitation not disclosed in Watt of:

> "forming at least one other well and threshold implantation into the other of the array and periphery areas of the semiconductor substrate"

The Examiner states in the Office Action dated June 14, 2005:

> "...and further including forming another well and threshold implantation into the other of the array and periphery areas over the semiconductor substrate (Figure 13)."

However, neither in Figure 13 nor anywhere else does Watt disclose forming at least one other threshold implantation into the other of the array and periphery areas of the semiconductor substrate.

With regard to one region, region 108, Watt does disclose threshold adjustment, at column 8, lines 13–15:

> "...channel dopant region 118 may serve to adjust the threshold of a subsequently formed p-channel transistor."

However, with regard to all other regions that are disclosed or discussed, there is no mention or disclosure of threshold adjustment or of threshold implantation. For example, with regard to region 134, Watt states only, at column 9, lines 45–59:

> "[C]hannel impurities 132 may be introduced into patterned layer 128 and exposed region 130 to form channel dopant region 134 within well 122 as illustrated in FIG. 9. Preferably, channel impurities 132 are of the same conductivity type as well impurities 120. As such, channel impurities 132 may be of opposite conductivity type to well impurities 112 and channel impurities 116. The introduction of channel impurities 132 may form channel dopant region 134 with a peak concentration between approximately 2.0×10^{16} cm^{-3} and approximately 2.0×10^{18} cm^{-3} and depth between approximately 0.05 microns and approximately 0.25 microns. Channel dopant regions with larger or smaller depths and concentrations, however, may be formed depending on the design specifications of the device." [underlining for clarity]

There is no mention above of threshold implantation. Thus, Watt does not disclose forming at least one other threshold implantation into the other of the array and periphery areas of the semiconductor substrate as now claimed in claim 1.

It is therefore respectfully submitted that independent claim 1, and the respective claims 2 and 5 depending therefrom, are not anticipated by Watt under 35 USC §102(a) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejection is therefore respectfully requested.

Regarding claims 2 and 5, these dependent claims each depend from independent claim 1 and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejection of claims 2 and 5 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Claim Rejections - 35 USC §103

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US Patent Application Publication US 2003/00232472 Al, hereinafter "Wu") in view of Watt (U. S. Patent 6,586,296 B1, hereinafter "Watt").

Watt was previously summarized above.

Wu provides methods of fabricating a stack-gate non-volatile memory device and its contactless memory arrays. A stack-gate non-volatile memory device with a tapered floating-gate structure is disclosed in which the tapered floating-gate structure offers a longer effective channel length to alleviate the punch-through effect and a larger surface area for erasing or programming between the tapered floating-gate structure and the integrated common-source/drain conductive structure. The stack-gate non-volatile memory devices are implemented into three contactless array architectures: a contactless NOR-type array, a contactless NAND-type array, and a contactless parallel common-source/drain conductive bit-lines array.

Regarding claim 6, the Applicants respectfully traverse the rejection on the grounds that the Applicants' claimed combination would not be unpatentable over Wu in view of Watt since the Applicants' claimed combination includes the limitation of:

"forming an oxide-nitride-oxide dielectric layer on the semiconductor substrate"

The Examiner states in the Office Action:

> "forming an oxide-nitride-oxide dielectric layer 301 on the semiconductor substrate"

However, Wu does not teach or suggest forming an oxide-nitride-oxide dielectric layer on the semiconductor substrate, but rather in paragraph [0036] states:

> "The first gate-dielectric layer 301 is preferably a thermal-oxide layer or a nitrided thermal-oxide layer having a thickness between 80 Angstroms and 120 Angstroms." [underlining for clarity]

The above shows that Wu's layer 301 is not, and does not describe, teach, or suggest, a three layer, oxide-nitride-oxide dielectric layer. Thus, the layer 301 is not an oxide-nitride-oxide dielectric layer on the semiconductor substrate. Withdrawal of the rejection is therefore respectfully requested because:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) [underlining for clarity]

Accordingly, and based upon the above, it is respectfully submitted that independent claim 6 is allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art. Allowance thereof on this ground is therefore respectfully requested.

The Examiner additionally stated that

> "It would have been obvious ... since ... it will ... enable NMOS and PMOS transistors to be formed on the same substrate." [deletions for clarity]

However, the Examiner has not shown or cited a section in either Wu or Wart that would support the above statement. Thus, no motivation has been presented for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in either reference any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Wu in view of Watt cannot be maintained, and independent claim 6 is accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1, 2, and 5–10 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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